IN THE CLAIMS:

Please amend claims 1, 3 and 4, cancel claim 2, and add new claims 13-18 as follows:

1. (Currently Amended) A semiconductor device comprising:

a plurality of memory cells coupled to a plurality of word lines and a plurality of data lines; and

a plurality of word drivers controlling voltages (SWL) applied to said plurality of word lines,

wherein a voltage applied to one of said plurality of word lines for a read operation is lower than a voltage applied to one of said plurality of word lines for a write operation,

wherein said voltage applied to one of said plurality of word lines for said read operation is higher than a voltage applied to one of said plurality of word lines which are not selected for either said read operation or said write operation, and

wherein said plurality of memory cells each comprises at least a transistor having a gate coupled to said one of said plurality of word lines, and having a source/drain path between one of said plurality of data lines and a node supplied with a predetermined voltage.

2. (Canceled)

3. (Currently Amended) The semiconductor device according to claim ~~2~~ 1,

wherein a voltage applied to said plurality of word lines during a recharge operation is lower than a ground voltage.

4. (Currently Amended) The semiconductor device according to claim 1,

wherein said voltage applied to one of said plurality of word ~~liens~~ lines for said read operation is lower than a voltage of one selected data line of said plurality of data lines.

5. (Previously Presented) The semiconductor device according to claim 4,

wherein said voltage applied to one of said plurality of word lines for said write operation is higher than said voltage of one selected data line of said plurality of data lines.

6. (Previously Presented) The semiconductor device according to claim 5, wherein said plurality of memory cells are dynamic memory cells.

7. (Previously Presented) A semiconductor device comprising:

a plurality of memory cells coupled to a plurality of word lines and a plurality of data lines; and

a plurality of word drivers controlling voltages (SWL) applied to said plurality of word lines,

wherein a voltage applied to a selected word line of said plurality of word lines for a read operation is lower than a voltage applied to a selected word line of said plurality of word lines for a write operation,

wherein said voltage applied to said selected word line of said plurality of word lines for read operation has a positive value.

8. (Previously Presented) The semiconductor device according to claim 7, wherein said voltage applied to said selected word line of said plurality of word lines for said read operation is higher than a voltage applied to said plurality of word lines for a recharge operation.

9. (Previously Presented) The semiconductor device according to claim 8, wherein said plurality of memory cells each comprises at least a transistor having a gate coupled to said one of said plurality of word lines, and having a source/drain path between one of said plurality of data lines and a node supplied with a predetermined voltage.

10. (Previously Presented) The semiconductor device according to claim 9, wherein a voltage pplied to said plurality of word lines during said recharge operation has a negative value.

11. (Previously Presented) The semiconductor device according to claim 10, wherein said voltage applied to said selected word line of said plurality of word lines for said read operation is lower than a voltage of a selected data line of said plurality of data lines.

12. (Previously Presented) The semiconductor device according to claim 11,

wherein said voltage applied to said selected word line of said plurality of word lines for said write operation is higher than said voltage of said selected data line of said plurality of data lines.

13. (New) A semiconductor device comprising:

a plurality of memory cells coupled to a plurality of word lines and a plurality of data lines; and

a plurality of word drivers controlling voltage applied to said plurality of word lines;

wherein a first voltage applied to one of said plurality word lines for a read operation is lower than a second voltage applied to one of said plurality of word lines for a write operation,

wherein said first voltage is higher than a third voltage applied to one of said plurality of word lines which are not selected for either said read operation or write operation,

wherein each of said plurality of word drivers includes a first MOS transistor having a source and a drain which are coupled between a corresponding one of said plurality of word lines and said first voltage, a second MOS transistor having a source and a drain which are coupled between a corresponding one of said plurality of word lines and said second voltage, and a third MOS transistor having a source and a drain which are coupled between a corresponding one of said plurality of word lines and said third voltage.

14. (New) The semiconductor device according to claim 13, wherein said plurality of memory cells each comprises at least a transistor having a gate coupled to said one of said plurality of word lines, and having a source/drain path between one of said plurality of data lines and a node supplied with a predetermined voltage.

15. (New) The semiconductor device according to claim 13,

wherein a voltage applied to said plurality of word lines during a recharge operation is lower than a ground voltage.

16. (New) The semiconductor device according to claim 14,

wherein said voltage applied to one of said plurality of word lines for said read operation is lower than a voltage of one selected data line of said plurality of data lines.

17. (New) The semiconductor device according to claim 15,

wherein said voltage applied to one of said plurality of word lines for said write operation is higher than said voltage of one selected data line of said plurality of data lines.

18. (New) The semiconductor device according to claim 16,

wherein said plurality of memory cells are dynamic memory cells.